What is Claimed is:

1. A method for fabricating a high voltage dual gate device comprising:

forming high voltage n-type and p-type well regions in a high voltage device forming region of a semiconductor substrate, the substrate also having a low voltage device forming region;

forming the source/drain of a high voltage NMOS transistor and the source/drain of a high voltage PMOS transistor in the well regions;

forming a trench by a STI process and forming a device isolation layer in the trench and forming a buffer nitride film on the resulting structure;

forming a high voltage gate oxide film on the buffer nitride film and etching portions of the high voltage gate oxide and buffer nitride films disposed over the low voltage device forming region leaving the said high voltage gate oxide and buffer nitride films intact on top of the high voltage device forming region; and

forming low voltage p-type and n-type well regions in the low voltage device forming region and forming a low voltage gate oxide film on top of the low voltage device forming region.

2. The method of claim 1, wherein, in the etching of the high voltage gate oxide film and buffer nitride film, the device isolation layer disposed over the high voltage device forming region is effectively protected from etching by the buffer nitride film.

3. The method of claim 1, wherein the device isolation layer is formed by depositing a HDP oxide film and then planarizing the HDP oxide film by a CMP process.

4. The method of claim 1 further comprising forming a gate electrode on top of the low voltage gate oxide layer and forming a gate electrode on the high voltage gate oxide film.

5. The method of claim 4, wherein said gate electrodes are formed from device driving gate polysilicon layers.

6. The method of claim 1, wherein the high voltage n-type and p-type well regions are formed by a drive-in diffusion process.

7. The method of claim 1, wherein the source/drain of the high voltage NMOS transistor and the source/drain of the high voltage PMOS transistor are formed by an ion implantation process and are subsequently drive-in diffused by annealing.

8. The method of claim 1, wherein the forming of the trench by the STI process extends through a buffer oxide film, a planarization stop layer nitride film and a photoresist pattern.

9. The method of claim 1, wherein the buffer nitride film has a thickness of less than or about 300 Å.

10. The method of claim 1, wherein the high voltage gate oxide film has a thickness of about 1,000 Å.

11. The method of claim 2, wherein the device isolation layer is formed by depositing a HDP oxide film and then planarizing the HDP oxide film by a CMP process.

12. The method of claim 11 further comprising forming a gate electrode on top of the low voltage gate oxide layer and forming a gate electrode on the high voltage gate oxide film.

13. The method of claim 12, wherein said gate electrodes are formed from device driving gate polysilicon layers.

14. The method of claim 13, wherein the high voltage n-type and p-type well regions are formed by a drive-in diffusion process.

15. The method of claim 14, wherein the source/drain of the high voltage NMOS transistor and the source/drain of the high voltage PMOS transistor are formed by an ion implantation process and are subsequently drive-in diffused by annealing.

16. The method of claim 15, wherein the forming of the trench by the STI process extends through a buffer oxide film, a planarization stop layer nitride film and a photoresist pattern.

17. The method of claim 16, wherein the buffer nitride film has a thickness of less than or about 300 Å.

18. The method of claim 17, wherein the high voltage gate oxide film has a thickness of about 1,000 Å.

19. A method for fabricating a high voltage dual gate device comprising:

providing a semiconductor substrate having a high voltage device forming region and a low voltage device forming region;

forming a trench in the high voltage device forming region;

forming a device isolation layer in the trench;

forming a buffer nitride film on the device isolation layer;

forming a high voltage gate oxide film and buffer nitride film on the resultant structure and etching portions of the high voltage gate oxide and buffer nitride films disposed on top of the low voltage device forming region of the semiconductor substrate thereby leaving the high voltage gate oxide film and buffer nitride films intact on top of the high voltage device forming region; and

forming low voltage p-type and n-type well regions in the low voltage device forming region and forming a low voltage gate oxide film on top of the low voltage device forming region.

20. The method of claim 19, wherein the device isolation layer is formed by depositing an HDT oxide film and then planarizing said HDT oxide film by a CMP process.